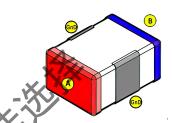


■ DESCRIPTION

When used in balanced line applications, the revolutionary design provides simultaneous line-to-line and line-to-ground filtering, using a single ceramic chip. In this way, differential and common mode filtering are provided in one device. For unbalanced applications, it provides ultra low ESL (equivalent series inductance). Capable of replacing 2 or more conventional devices, it is ideal for balanced and unbalanced lines.

The BDL(Balanced Dual-Line) device performs as a broadband filter enabling better EMC compliance for electrical equipment in a wide range of applications.



■ FEATURE

BDL is effective up to 10GHz and frequencies beyond.

Noise cancellation within BDL makes ESL reducing from nH to pH levels.

Unlike feed through capacitors, BDL is in bypass, so no DC current limitations.

Two tightly matched line to ground capacitors in one device.

■ ADVANTAGES

- Replace up to 7 components with one BDL
- Matched capacitance line to ground, both lines
- One device for EMI suppression or decoupling
- Differential and common mode attenuation
- Low inductance due to cancellation effect

■ APPLICATIONS

- Amplifier Filter & Decoupling
- DDR Memory
- High Speed Data Filtering
- FPGA/ASIC Decoupling
- DC Motor



■ QUICK REFERENCE DATA

DESCRIPTION	VALUE
Rated voltage	500V
SRF	110MHz
Insulation Resistance	IR>500 Ω •F or 10G Ω whichever is less Measurement at 25 °C ,WVDC,time is 2 minutes max.
Dissipation Factor	≤2.5%(0.025)
Dielectric Strength	1.5×WVDC,25 C
Operating temperature range	-55 C to +125 C
Test voltage(DC)for 1 minute	1.5×UR
Capacitance(A/B)	5000pF±20%

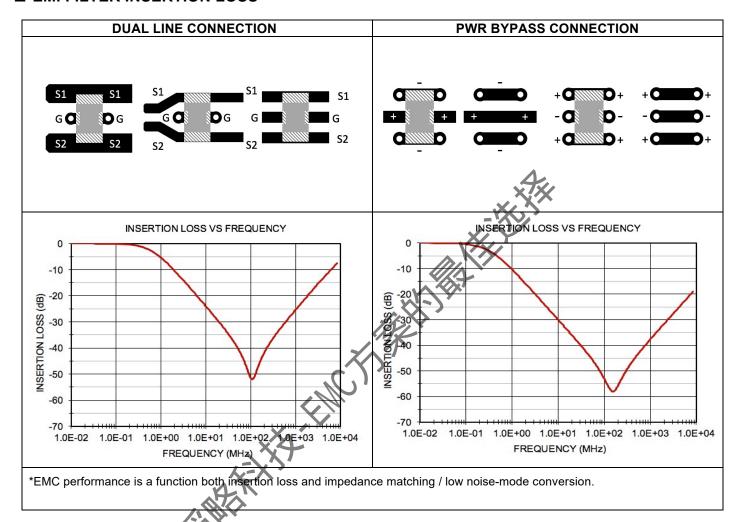
JOPF **■ DEVICE ORDERING INFORMATION** BDL1210S110V501T Packing: Tape & Reel Rated voltage V500=50V V101=100V V501=500V SRF: 110MHz Size code EIA mm 0603 (1608M) 0805 (2012M) (3216M) (3225M) (3625M) 1206 1210 1410

BDL EMI FILTER



B**DL EMI F**ilter

■ EMI FILTER INSERTION LOSS



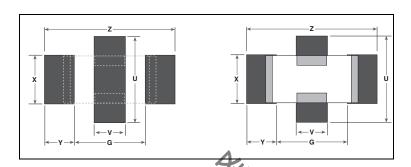
SIZE	IN	(mm)	L
L	0.125±0.010	3.175±0.254	
W	0.098±0.010	2.489±0.254	<u>↑</u>
Т	0.070max	1.778max	w †
EB	0.018±0.010	0.457±0.254	C/L OF CHIP ↓ ↓
СВ	0.045±0.005	1.143±0.127	w _B
WB	0.006±0.005	0.152±0.100	→ EB ← ' ← CB → ← EC →



B**DL EMI F**ilt**er**

■ SOLDER PAD RECOMMENDATIONS:

	SOLDER REFLOW		
	IN	mm	
X	0.100	2.54	
Υ	0.040	1.02	
G	0.080	2.03	
V	0.045	1.14	
U	0.160	4.06	
Z	0.160	4.06	



■ SOLDER PROCESS RECOMMENDATIONS:

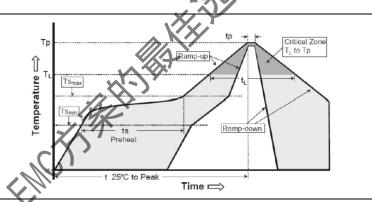
SOLDER REFLOW:

Recommended temperature profiles for reflow soldering are shown in Table 1 and Figure 1 from J-STD-020C

Preheat ramp: 1-3°C/sec.

Preheat: 75-125°C < T (max)

T (max): 210-260°C



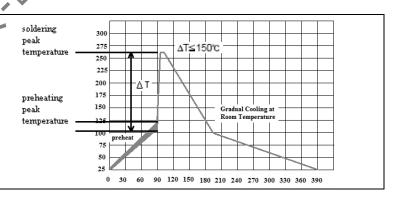
SOLDER WAVE: Caution, NOT recommended for sizes >1206

Preheat Temp.:100-120°C

Δ T Pre-Heat: 150°C max

Soldering Peak Temp.: 250-260°C, 5 SEC max.

Cool Down: <2°C/SEC



SOLDERING NOT SUPPORTED FOR USE IN MASS

Not recommended for lab proto-typing, use solder reflow, hot-air tool, or conductive epoxy to thermal damage and compromised test results. If Iron is used, follow below

- Preheat circuit and capacitors to within 100° C of soldering
- · No contact of iron tip with
- 20 watt iron output
- 350° C tip temperature
- 1.0 mm tip diameter
- Limit soldering time to 3 sec.